AMENDMENTS TO THE SPECIFICATION:

Please delete the word "Description" at page 1, line 1.

Please add the following centered heading at page 1, line 5:

TECHNICAL FIELD

Please add the following centered heading at page 1, line 15:

BACKGROUND

Please add the following centered heading at page 2, line 15:

SUMMARY

Please add the following centered heading at page 4, line 5:

DESCRIPTION OF THE DRAWINGS

Please add the following centered heading at page 4, line 18:

DETAILED DESCRIPTION

Please replace the paragraph beginning at page 1, line 6 with the following amended paragraph:

A ~~The invention relates to a~~ circuit arrangement for protecting integrated semiconductor circuits from electrical pulses or electrical overvoltages is disclosed.

Please replace the paragraph beginning at page 3, line 30 with the following amended paragraph:

In some embodiments, ~~The invention is based on the object of specifying~~ an active protection circuit ~~which~~ exhibits a response which is, in contrast, improved.

Please delete the paragraph beginning "The invention achieves this object" at page 3, line 34.

Please replace the paragraph beginning at page 4, line 35 with the following amended paragraph:

The resistor R1, together with the capacitor ~~capacitance~~ C1, forms an RC element. The resistor R1 is preferably in the form of a diffusion resistance and the capacitor ~~capacitance~~ C1 is preferably in the form of an oxide or gate oxide capacitance.

Please replace the paragraph beginning at page 5, line 36 with the following amended paragraph:

The resistor R1, together with the capacitor ~~capacitance~~ C1, forms an RC element. The resistor R1 is preferably in the form of a diffusion resistance and the capacitor ~~capacitance~~ C1 is preferably in the form of an oxide or gate oxide capacitance.

Please replace the paragraph beginning at page 6, line 10 with the following amended paragraph:

In some embodiments, ~~According to the invention,~~ the described problems such as the tendency to oscillate and oversensitivity to EMC can be eliminated using pull-up and pull-down resistors which are appropriately dimensioned and are introduced at a suitable point in the above-described ESD protection circuit, in particular the inverter chain. In this case, the pull-up and pull-down resistors are connected to the supply potential and/or reference ground potential. As a result, the switch-on speed of circuits which are protected in this manner may, in turn, be increased for running up the supply voltage.

Please replace the Abstract on page 12 with the following new Abstract:

A circuit arrangement includes an RC element connected between a first supply potential line and a second supply potential line. The RC element includes a first resistor and a first capacitor. The circuit arrangement also includes a plurality of inverters connected in series and having junction points between the inverters in the plurality of inverters. An input of the plurality of inverters is connected to a point between the first resistor and the first capacitor. The circuit arrangement also includes a protection transistor and a plurality of resistors.

Please delete the phrase " Active protection circuit arrangement" at page 12, line 4.

Please delete the phrase " Figure 2" at page 12, line 22.